

**Storage Solution for Marvell's PXA300/310 platform
Users Manual
v1.0**

Arasan Chip Systems Inc.

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1. GLOSSARY

1.1 Definitions

Term	Definition
SDIO Bus Driver Stack	This covers the SDIO protocol and Host Controller Driver functions like device enumeration, initialization and configuration.

Table 1: Definitions

1.2 Abbreviations

Abbreviation	Expansion
SDIO	Smart Digital Input Output
SD	Secure Digital
MMC	Multi Media Card
ATA	Advanced Technology Attachment
CE-ATA	Consumer Electronics Advanced Technology Attachment
SD	Secure Digital

Table 2: Abbreviations

2. INTRODUCTION

2.1 Purpose

This document describes the user level access to the storage interface board for Marvell's PXA300/310 handheld platform kit.

3. HARDWARE & SOFTWARE SETUP

3.1 Hardware Details

The following hardware is required

- Marvell's PXA300/310 handheld platform
- Arasan VLIO-SD/SDIO Host Controller Card
- SD/MMC Memory cards

3.2 Interfaces Supported

ACTEL Tiger supports:

- SDIO/MMC Slot
- Micro SD Slot
- CE-ATA 4 bit interface
- CE-ATA 8 bit interface

3.3 Setup Diagram

Littleton Development Board – This development board is a combination of following two modules.

- **Littleton Main Board**
This is the main board with the PXA300 processor.
- **Actel Igloo Board**
This board is the Arasan's VLIO SD-Host Controller card for SD/MMC/SDIO/CE-ATA.



3.4 Software Details

The Littleton Actel Igloo Board has following software components:

1. Qtopia linux having kernel 2.6 running on Littleton
2. Bit File programmed to the FPGA
3. Nex Bus driver

4. SYSTEM STARTUP

On powering up the Littleton Actel Igloo device the NexBus driver will load automatically while the linux kernel boots. Whenever a SD/MMC card is inserted into the slot it is automatically detected and a storage folder appears for it. Similarly whenever a SD/MMC card is removed from the slot, its removal is handled properly and the storage folder disappears.

5. RUNNING SLIDE SHOW

- Insert a SD/MMC card into the slot. On insertion, a storage folder appears.
- Go to the Applications tab, click on the 'Pictures' application.
- Go to the File menu and click on Open and browse to the storage folder.
- Select all the *.gif files.
- Go to the Run Menu and click on slide show.
- The slide show of the pictures will start.

6. RUNNING MP3 FILES

- Insert a SD/MMC card having MP3 files into the slot. On insertion, a storage folder appears.
- Go to Applications tab, click on the 'Music' application
- Go to File Menu and click on Open and then browse to the storage folder.
- Select a single or multiple MP3 files.
- Right click on selected files and select the Play option.
- The MP3 files start playing

7. APPENDIX

7.1 Actel Igloo Hardware

ACTEL Tiger is a reference design for low power ACTEL IGLOO AGL600-FG256 FPGA. ACTEL Tiger is a daughter board which is directly pluggable into LITTLETON Handheld unit expansion slot. The purpose of this document to display various interfaces and to measure current used by ACTEL IGLOO device in active and in Flash Freeze states.

7.1.1 Interfaces Supported:

ACTEL Tiger supports:

1. J19 - SDIO/MMC Slot
2. J21 - Micro SD Slot
3. J22 - CE-ATA 4 bit interface
4. J20 - CE-ATA 8 bit interface.

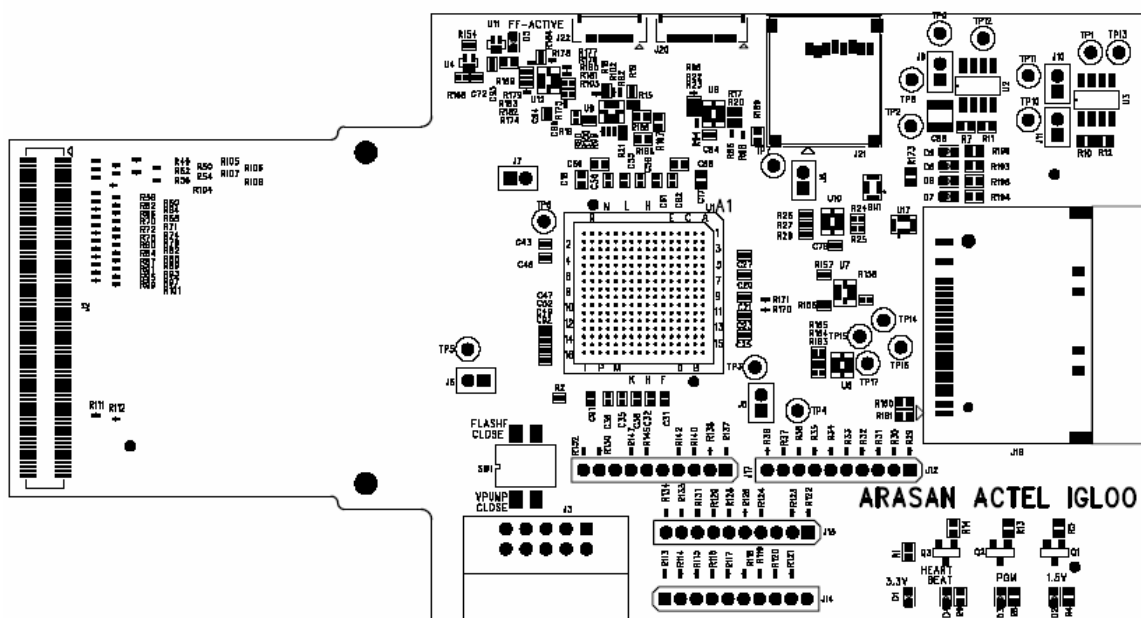


Figure 1: Storage Interface Daughter Board

7.1.2 LITTLETON Interface

The storage solution board interfaces with LITTLETON Handheld unit using J1 connector. Other daughter cards may be placed behind ACTEL Tiger daughter board using J2 connector. J1 and J2 are interconnected.

7.1.3 Programming Interface

J3 is a JTAG Interface for programming the ACTEL IGLOO Part. This interface accepts a standard FLASHPRO JTAG Cable. While programming it is essential that SW1-1 is close. This switch provides VPUMP 3.3V required for programming the ACTEL IGLOO part.

7.1.4 Standard SD/MMC Connector

J19 is a standard SD/MMC connector capable of accepting SD, Mini-SD, MMC and MMC-RS cards. This interface supports 8Bit MMC/MMC-RS cards.

7.1.5 Micro SD Connector

J21 is a Micro SD connector for Micro SD cards.

7.1.6 4 Bit CE-ATA

J22 is a 4 Bit CE-ATA connector to interface with 4 Bit CE-ATA Devices.

7.1.7 8 Bit CE-ATA

J20 is 8 Bit CE-ATA Connector to support 8 Bit CE-ATA devices.

7.1.8 Setting Core Voltage

ACTEL Tiger supports 1.2V or 1.5V VCC (Core Voltage). With Vcc=1.2V IGLOO operates at a lower clock rate but in low power mode. For 1.5V J11 should be open.

VCC = 1.2V	J11 JUMPERED
VCC = 1.5V	J11 NO JUMPER

Table 3: Setting for CORE Voltage

7.1.9 Current Measurements

ACTEL Tiger allows independent Core current and VBx Current measurements.

Total Core Current

Total Core Current can be measured by placing a meter between TP10 and TP11. Power down ACTEL Tiger. Ensure that the meter is correctly set to measure current. By removing jumper J10, the current will flow thru the meter for measurements.

VCC	J11	J10	Measured Current
VCC = 1.2V	J11 JUMPERED	Removed	
VCC = 1.5V	J11 NO JUMPER	Removed	

Table 4: Total Core Current

Total 3.3V Current

Total 3.3V current measurement allows measurement of total current drawn from 3.3V regulator.

Power down ACTEL Tiger. Place a current measuring meter between TP8 and TP9. Remove Jumpers J9. Power up ACTEL Tiger and measure 3.3V regulator Current. Power down and ensure J9 has a jumper in place for remaining tests.

Bank Current Measurements

To measure IO current per Bank following setup is required.

- Power down ACTEL Tiger. Place a current measuring meter between TP3 and TP4. Remove Jumpers J5, J6, J7 and J8. Power up ACTEL Tiger and measure total bank IO Current.
- Power down ACTEL Tiger. Place Jumpers J6, J7 and J8. Power up ACTEL Tiger and measure Bank0 IO Current.
- Power down ACTEL Tiger. Place Jumpers J5, J7 and J8. Power up ACTEL Tiger and measure Bank1 IO Current.
- Power down ACTEL Tiger. Place Jumpers J5, J6, and J8. Power up ACTEL Tiger and measure Bank2 IO Current.
- Power down ACTEL Tiger. Place Jumpers J5, J6, J7. Power up ACTEL Tiger and measure Bank3 IO Current.

VCC	Total IVbx	IVb0	IVb1	IVb2	IVb3
VCC=1.2V					
VCC=1.5V					

Table 5: Bank IO Current

7.1.10 IGLOO FLASH FREEZE Function

ACTEL IGLOO FLASH FREEZE function may be activated by closing SW1-2 switch. This function shows the currents may be reduced significantly when IGLOO is operating in a flash freeze mode.

Repeat instructions in section 1.1.8 for Flash Freeze mode current measurements.

LED Functions

D1	3.3V OK
D2	1.5V OK
D3	IGLOO VPUMP Active
D4	IGLOO HEART BEAT 500ms Pulse
D5	IGLOO Flash Freeze Active
D6	8bit CEATA VDD Active
D7	SD VDD Active
D8	4Bit CEATA VDD Active
D9	Micro SD VDD Active

Table 6: LED Functions

Variable Length IO Interface

Variable Length IO Interface is the major interface from LITTLETON to ACTEL IGLOO device. This section describes the connectivity from expansion connector to IGLOO.

DF_ALE_WE_N	U1.R6	J2.10	J1.10
DF_BE0	U1.R5	J2.4	J1.4
DF_BE1	U1.T5	J2.5	J1.5
DF_CLE_OE_N	U1.P6	J2.9	J1.9
DF_INT_RNB	U1.N8	J2.16	J1.16
DF_IO_0	U1.P8	J2.17	J1.17
DF_IO_1	U1.R8	J2.18	J1.18
DF_IO_2	U1.T8	J2.19	J1.19
DF_IO_3	U1.T9	J2.20	J1.20
DF_IO_4	U1.R9	J2.21	J1.21
DF_IO_5	U1.P9	J2.22	J1.22
DF_IO_6	U1.N9	J2.23	J1.23
DF_IO_7	U1.M9	J2.24	J1.24
DF_IO_8	U1.T10	J2.25	J1.25
DF_IO_9	U1.R10	J2.26	J1.26
DF_IO_10	U1.P10	J2.27	J1.27
DF_IO_11	U1.T11	J2.28	J1.28
DF_IO_12	U1.N10	J2.29	J1.29
DF_IO_13	U1.R11	J2.30	J1.30
DF_IO_14	U1.T13	J2.31	J1.31
DF_IO_15	U1.P11	J2.32	J1.32
DF_LLA_N	U1.T6	J2.11	J1.11
DF_LUA_N	U1.N7	J2.12	J1.12
DF_OE_N	U1.R7	J2.14	J1.14
DF_RDY	U1.T7	J2.15	J1.15
DF_SCLK	U1.A2	J2.7	J1.7
DF_WE_N	U1.P7	J2.13	J1.13

Table 7: VLIO Interface

R_M_RESET_IN	U1.A4
R_M_RESET_O	U1.C5
TECH_CS0_N	U1.T2
TECH_CS1_N	U1.T4
TECH_DF_CS_N	U1.P5
TECH_INT_1_N	U1.L14
TECH_INT_2_N	U1.L15
TECH_INT_3_N	U1.L16
TECH_INT_4_N	U1.M16

Table 8: LITTLETON Interrupt Interface

JTAG Interface

ACTEL IGLOO JTAG interfaces with FLASHPRO programmer using J3 connector.

IG_TCK	U1.P13	J3.1
IG_TDI	U1.R14	J3.9
IG_TDO	U1.R16	J3.3
IG_TMS	U1.T15	J3.5
IG_TRST	U1.P15	J3.8
IG_VPUMP	U1.P14	J3.7

Table 9: JTAG Interface

CE-ATA 8bit IGLOO Interface

Following signals connect to ACTEL IGLOO for CE-ATA.

CEATA_CLK	U1.E1	J20.10
CEATA_CMD	U1.D2	J20.8
CEATA_DAT0	U1.F1	J20.15
CEATA_DAT1	U1.F2	J20.16
CEATA_DAT2	U1.E4	J20.2
CEATA_DAT3	U1.D1	J20.3
CEATA_DAT4	U1.C2	J20.5
CEATA_DAT5	U1.C1	J20.6
CEATA_DAT6	U1.E3	J20.12
CEATA_DAT7	U1.F4	J20.13
CEATA_PWREN	U1.E8	
CEATA_VDD		J20.7
CEATA_VIO		J20.9

Table 10: CEATA Connectivity

CE-ATA 4bit IGLOO Interface

Additional 4 Bit CE-ATA Interface is provided to attach a 4 Bit CEATA device.

CEA_CLK	U1.J4	J22.7
CEA_CMD	U1.K2	J22.5
CEA_DAT0	U1.L1	J22.9
CEA_DAT1	U1.K3	J22.10
CEA_DAT2	U1.G2	J22.2
CEA_DAT3	U1.G1	J22.3
CEA_PWREN	U1.C9	
CEA_VDD		J22.4

Table 11: 4Bit CEATA Connector

Micro SD Interface

J21 is provided for Micro SD interface. This interfaces to ACTEL IGLOO using following pins.

USD_CD/DAT3	U1.M1	J21.2
USD_CLK	U1.L4	J21.5
USD_CMD	U1.N1	J21.3
USD_DAT0	U1.N2	J21.7
USD_DAT1	U1.M3	J21.8
USD_DAT2	U1.L2	J21.1

USDCD	U1.D9	J21.9
USD_PWREN	U1.A9	

Table 12: Micro SD Connectivity

I2C Interface to LITTLETON

I2C_SCL	U1.G15	J1.96	J2.96
I2C_SDA	U1.G16	J1.95	J2.95

Table 13: I2C Connectivity

SD/MMC Interface

SD/MMC is a multi-function connector supporting standard SD or MMC cards as well as Mini-SD and MMC-RS cards.

CLK_PORT1	U1.C13	J19.11	J19.15
CMD_PORT1	U1.B5	J19.20	J19.7
DAT0_PORT1	U1.A12	J19.18	J19.5
DAT1_PORT1	U1.D11	J19.19	J19.3
DAT2_PORT1	U1.C11	J19.4	J19.22
DAT3_PORT1	U1.B11	J19.21	J19.6
DAT4_PORT1	U1.A11	J19.23	C88.1
DAT5_PORT1	U1.D10	J19.24	R164.2
DAT6_PORT1	U1.C10	J19.25	R163.2
DAT7_PORT1	U1.B10	J19.26	R162.2
SDCD_PORT1	U1.A10	J19.2	
SDWP_PORT1	U1.E9	J19.1	

Table 14: SD/MMC Connectivity

IGLOO Normal IO Debug Connections

Following pins are available as normal IO pins.

DBGR1	U1.A5	J12.1
DBGR2	U1.D6	J12.2
DBGR3	U1.B6	J12.3
DBGR4	U1.A6	J12.4
DBGR5	U1.A7	J12.5
DBGR6	U1.B7	J12.6
DBGR7	U1.C7	J12.7
DBGR8	U1.D7	J12.8
DBGR9	U1.A8	J12.9
DBGR10	U1.B8	J12.10
DBGR24	U1.G14	J14.1
DBGR25	U1.E14	J14.2
DBGR26	U1.E16	J14.3
DBGR27	U1.F16	J14.4
DBGR28	U1.C16	J14.5

DBGR29	U1.D16	J14.6
DBGR30	U1.F13	J14.7
DBGR31	U1.C15	J14.8
DBGR32	U1.B16	J14.9

Table 15: IGLOO General IO Debug Pins

IGLOO Global Resources

Following Debug pins are connected to Global resource pins for testing purposes.

GRR1	U1.B15	J15.1
GRR10	U1.G13	J17.1
GRR11	U1.J14	J17.2
GRR12	U1.P16	J17.3
GRR13	U1.N16	J17.4
GRR14	U1.L13	J17.6
GRR15	U1.M14	J17.7
GRR16	U1.N15	J17.9
GRR17	U1.M15	J17.10
GRR2	U1.D14	J15.2
GRR3	U1.E13	J15.4
GRR4	U1.H14	J15.5
GRR5	U1.J13	J15.6
GRR6	U1.J16	J15.7
GRR7	U1.H16	J15.8
GRR8	U1.H13	J15.9
GRR9	U1.J12	J15.10

Table 16: IGLOO Global resource pins